PCT WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 5 : H04B 1/06 — A1

(11) International Publication Number: WO 90/14718

(43) International Publication Date: 29 November 1990 (29.11.90)

(21) International Application Number: PCT/US90/02301

(22) International Filing Date: 30 April 1990 (30.04.90)

(30) Priority data:
353,725 — 18 May 1989 (18.05.89) — US
439,303 — 21 November 1989 (21.11.89) — US

(71) Applicant: MOTOROLA, INC. [US/US]; 1303 East Algonquin Road, Schaumburg, IL 60196 (US).

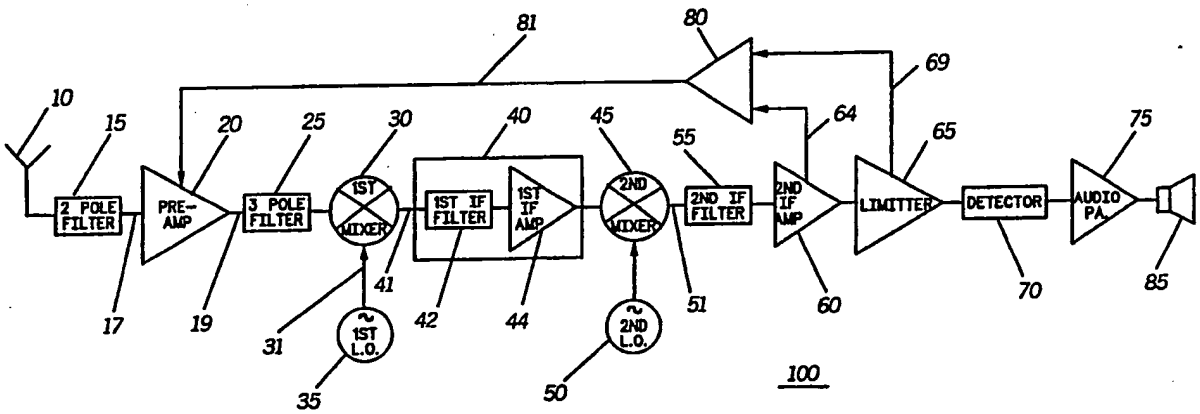
(72) Inventors: RUELKE, Charles, R. ; 320 NW 135th Avenue, Planatation, FL 33325 (US). FRASER, Randall, S. ; 6170 SW 44th Street, Davie, FL 33314 (US).

(74) Agents: PARMELEE, Steven, G. et al.; Motorola, Inc., Intellectual Property Dept., 1303 East Algonquin Road, Schaumburg, IL 60196 (US).

(81) Designated States: AT (European patent), BE (European patent), CH (European patent), DE (European patent)*, DK (European patent), ES (European patent), FR (European patent), GB (European patent), IT (European patent), JP, LU (European patent), NL (European patent), SE (European patent).

Published
With international search report.

(54) Title: METHOD AND APPARATUS FOR REDUCING INTERMODULATION DISTORTION



(57) Abstract

A receiver (100) is provided having an amplifier (230) for amplifying a received RF signal. An Automatic Gain Control (AGC) circuitry (220) controls the gain of the amplifier, in response to a control signal (81) by changing the bias point of the amplifier. A Received Signal Strength Indicator (RSSI) circuitry provides the control signal (80), which is proportional to the strength of the received signal. As the strength of the received signal is increased the gain of the amplifer is decreased (and vice versa). The received signal bypasses the amplifier when the gain of the amplifier is reduced to a threshold level.

DESIGNATIONS OF "DE"

Until further notice, any designation of "DE" in any international application whose international filing date is prior to October 3, 1990, shall have effect in the territory of the Federal Republic of Germany with the exception of the territory of the former German Democratic Republic.

FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AT	Austria	ES	Spain	MC	Monaco
AU	Australia	FI	Finland	MG	Madagascar
BB	Barbados	FR	France	ML	Mali
BE	Belgium	GA	Gabon	MR	Mauritania
BF	Burkina Fasso	GB	United Kingdom	MW	Malawi
BG	Bulgaria	GR	Greece	NL	Netherlands
BJ	Benin	HU	Hungary	NO	Norway
BR	Brazil	IT	Italy	RO	Romania
CA	Canada	JP	Japan	SD	Sudan
CF	Central African Republic	KP	Democratic People's Republic of Korea	SE	Sweden
CG	Congo			SN	Senegal
CH	Switzerland	KR	Republic of Korea	SU	Soviet Union
CM	Cameroon	LI	Liechtenstein	TD	Chad
DE	Germany, Federal Republic of	LK	Sri Lanka	TG	Togo
DK	Denmark	LU	Luxembourg	US	United States of America

METHOD AND APPARATUS FOR REDUCING INTERMODULATION DISTORTION

Technical Field

This invention relates generally to the field of radio communication, and more particularly to a radio receiver having improved intermodulation and sensitivity.

Background Art

In a radio receiver, a received signal is often preamplified in a preamplifier stage. Saturation of the preamplifier stage under strong signal conditions typically increases nonlinearities in the preamplification thereby increasing intermodulation (IM). Also, strong signals at the preamplifier stage of a receiver can cause the preamplifier to oscillate, even though the preamplifier has been designed to satisfy a stability criteria under low level signal conditions. In attempting to eliminate the strong signal instability issues, optimization of small signal noise figure, gain, and input and output match are usually sacrificed, which degrades the receiver's sensitivity.

In order to minimize the problems associated with strong signal conditions, an automatic gain control (AGC) circuit may be used in conjunction with the preamplifier stage. Some AGC circuits provide a constant amplitude at the output of the preamplifier stage, by feeding back a control signal proportional to the preamplifier's signal output. However, the use of a

preamplifier stage having this type of AGC circuit does not compensate for variations occurring in the subsequent stages of the receiver, such as mixers, and IF amplifiers. Accordingly, a need exists for a receiver capable of preamplification without degrading IM performance.

Summary of the Invention

Accordingly, it is an object of the present invention to provide a receiver having improved intermodulation, and sensitivity.

It is another object of the present invention to provide a receiver having reduced current drain.

Briefly, according to the invention, a radio receiver is provided comprising a RF amplifier stage that varies the gain of the amplifier in response to a control signal. The control signal is preferably proportional to the received signal strength. The preamplifier stage also includes means for bypassing the amplifier when the gain of the amplifier is reduced to zero. When the amplifier stage is by passed, it may be inactivated or shut down so as to save reduce current drain in the radio receiver.

Brief Description of the Drawings

Figure 1 is block diagram of a radio receiver according to the present invention.

FIG 2a is block diagram of the 2nd IF amplifier stage of the receiver of FIG. 1.

FIG 2b is block diagram of the limiter stage of the receiver of FIG. 1.

Figure 3 is schematic diagram of the RF preamplifier stage of the receiver of Figure 1.

Detailed Description of the Preferred Embodiment

Referring to Figure 1, a block diagram of a double conversion FM receiver 100 is shown. The receiver 100 is preferably used in a portable two-way radio (not shown), and although a double conversion FM receiver is well known in the art, the stages and operation of the receiver 100 will be briefly described. In the preferred embodiment, the receiver 100 may be tuned to operate over the 935-941 MHZ band. Operationally, a signal received at the antenna 10 is coupled to a 2-pole filter 15. The 2-pole filter 15 provides the initial receiver selectivity, and produces a RF IN signal 17 proportional to the received signal. The RF IN signal 17 is applied to a preamplifier stage 20. As will be described latter, the preamplifier stage 20 may provide gain or may attenuate the received signal. An RF OUT signal 19, proportional to received signal, is provided by the preamplifier stage 20, and is applied to a 3-pole filter 25 to provide additional receiver selectivity. The 2-pole filter 15 and 3-pole filter 25 may be of any suitable type, such as, well known high Q dielectric resonator filters. The output of the 3-pole filter 25 and a 1st LO signal 31 are applied to a 1st mixer 30, and provides a 1st IF signal 41 at 39.15 MHZ. A 1st local oscillator source 35 provides the 1st LO signal, and may comprise a channel element (resonator) or may be a part of a phase locked loop frequency synthesizer. The 1st LO source is tuned to a proper frequency, so as to provide the proper 1st IF signal 41 when mixed with the RF OUT signal 19. The 1st mixer 30 may be of any suitable type having a non-liner characteristic. The output of the 1st mixer 30 is coupled to a first IF stage 40, which includes a 1st IF filter 42 and a 1st IF amplifier 44. The 1st IF filter 42 of the preferred embodiment comprises two 2-pole crystal band pass filters, each centered at the 1st intermediate frequency, and provide selectivity for the first IF stage 40. The output of the 1st IF filter is amplified by the 1st IF amplifier 44, and is coupled to a 2nd mixer 45. A 2nd LO

signal is applied to the 2nd mixer 45 by a 2nd LO source 50, and provides a 2nd IF signal 51 at 450 KHZ. The 2nd IF signal 51 is applied to a 2nd If filter 55, which preferably is a bandpass ceramic filter of suitable type centered at the 2nd intermediate frequency. The output of the 2nd IF filter 55 is amplified by a 2nd IF amplifier 60, and subsequently is limited by a limiter 65. The output of the limiter 65 is coupled to a FM detector 70, which recovers the modulating signal. The modulating signal, after amplification by an audio power amplifier 75, is coupled to a speaker 85. The detector 70, and the audio PA 75 may be of any suitable type, such as those used in the receiver section of a STX portable radio manufactured by Motorola, Inc.

Referring to FIG. 2a, the block diagram of the 2nd IF amplifier 60 is shown. The 2nd IF amplifier 60 includes two stages of cascaded amplifiers 61. The output of each amplifier is coupled to an RF detector 62, and each detector provides a DC signal representing the amplitude or strength of each stage. The detectors 61 may be any suitable RF detectors such as well known full wave or half wave rectifiers. In the preferred embodiment, the detectors 61 comprise temperature compensated full wave rectifiers. The output of the rectifiers 61 are summed by a summer 63, and the output 64 of the summer is a DC signal proportional to the signal strength the 2nd IF signal.

Referring to FIG. 2b, a block diagram of the limiter 65 is shown. The limiter 65 includes three cascaded limiting stages 66. The output of the limiting stages 66 are coupled to RF detectors 67, which are similar to RF detectors 62 of FIG. 2a. The DC outputs of the detectors 67 are summed by a summer 68, which provides a DC output 69 proportional to the strength of the 2nd IF signal.51.

Referring again to FIG. 1, the DC outputs 64 and 69 are coupled to a summer 80, which provides a DC received signal strength indicator (RSSI) output signal 81. Persons of ordinary

skill in the art will appreciate that the 2nd If signal strength is proportional to the received signal strength; therefore the RSSI signal 81 is proportional to the received signal strength Accordingly, as the strength of the received signal increases, the RSSI signal 81 will increase. Conversely, as the received signal strength decreases, the RSSI signal 81 will decrease. When each amplification or limiting stage is saturated, a maximum DC voltage will be provided by the RF detector corresponding to that stage, and each subsequent stage will provide additional DC voltage. Each stage will add a DC voltage proportional to its input signal thereby providing a relatively wide dynamic range for the RSSI signal 81. Persons of ordinary skill in the art will appreciate that the summer 80 of FIG. 1, summer 63 of FIG. 2a, and summer 69 of FIG. 2b may be replaced by a single summer to provide the RSSI signal 81. The RSSI signal 81 is applied to control the gain of the preamplifier stage 20. Accordingly, a negative feed back is provided, such that as the received signal strength is increased, the gain of the preamplifier stage 20 is decreased (even to zero where the preamplifier stage 20 is inactivated and bypassed, as will be described later).

Referring to FIG. 3 the schematic diagram of the preamplifier stage 20 of FIG. 1 is shown. A RF IN signal 17 proportional to the received signal of the receiver 100 of FIG. 1 is applied to an input matching network 211. The input matching network 211 provides the impedance matching to the previous stage to maximize power transfer into the preamplifier 20 (2-pole filter 15 of FIG. 1). The output of the matching network 211 is coupled to the base of an amplifier transistor 230. The output of the transistor amplifier 230 is provided at its collector, which is coupled to an output matching network 240. The output matching network 240 provides for the impedance matching to maximize power transfer to the subsequent stage (3-pole filter 25 of FIG. 1). The biasing circuitry for the transistor amplifier 230 includes a

resistor 225, coupled between the collector of the transistor amplifier 230 and a supply voltage Vs. The emitter of the transistor amplifier 230 is coupled to ground. Furthermore, a resistor 231 is coupled between the resistor 225 and the emitter of a PNP transistor 220. The collector of the transistor 220 is coupled to the base of the transistor amplifier 230 and a resistor 205 having its second terminal grounded. The base of the transistor 220 is coupled to the RSSI signal 81 through a resistor 215 and an inductor 221, and a resistor 217 and a capacitor 219 are coupled between the junction 216 and ground. The RSSI signal 81 provides for the controlling the bias of the transistor amplifier 230. As the RSSI signal 81 increases, the emitter voltage of the transistor 220 is increased, which reduces the current through the resistors, 205, 230, and 225. The reduction in current through resistor 205 drops the base voltage of the transistor amplifier 230 causing it to conduct less current, thereby reducing the gain of the transistor amplifier 230. The RSSI signal 81 may reach a level which causes the gain of the preamplifier stage 20 to become zero. At this point, the preamplifier stage 20 is shut down or inactivated, and the transistor amplifier 230 will present a very high impedance to the RF IN signal 17. Accordingly, the RF IN signal 17 bypasses the amplifier 230, and is routed via a inductor 235, and a capacitor 245 to the output matching network 240. The inductor 235, and the capacitor 245 comprise a passive bypass network 250. The transistor amplifier 230 is an active device, which significantly contributes to the generation of IM signals under strong signal condition. Therefore, passively bypassing the transistor amplifier 230 under strong received signal conditions greatly improves the IM performance of the receiver. Additionally, the passive network 250 may include attenuating means, such as a resistor divider to attenuate the received signal, thereby reducing the IM contribution of the subsequent active stages.

One of ordinary skill in the art may appreciate that the current drain of the preamplifier stage 20 reduces as the gain of the amplifier transistor 230 is decreased and reaches a minimum level when the preamplifier stage 20 is inactivated. Accordingly, under strong received signal conditions, wherein the preamplifier stage 20 is inactivated, the overall current drain of the receiver 100 is minimized prolonging its battery life.

Since the RSSI signal 81 is provided at the 2nd IF and is fully temperature compensated, the variations of the entire receiver front end are accounted for. Additionally, the stability considerations under strong signal conditions cause sacrificing the gain at low signal levels. Since the gain of the transistor amplifier 230 is reduced under strong signal conditions, the preamplifier stage 20 may be optimized to provide additional gain for low level received signals, thereby improving the receiver sensitivity.

What is claimed is:

Claims

1. A radio receiver, comprising:

means for receiving a signal to provide a received signal;

means for providing a control signal proportional to the strength of said received signal;

means for preamplifying said received signal, said preamplifying means include, an amplifier, means for automatically controlling the gain of said amplifier responsive to said control signal, and means for bypassing said amplifier when the gain of the amplifier is reduced to a threshold level.

2. The receiver of claim 1, wherein said automatic gain control means changes bias conditions of said amplifier.

3. The receiver of claim 1, wherein said means for bypassing attenuates said received signal.

4. The receiver of claim 1, wherein said receiver further includes, means for converting said received signal to an IF signal, said means for providing said control signal being proportional to the strength of said IF signal.

5. The receiver of claim 1, wherein said means for preamplifying is inactivated when the gain of the amplifier is reduced to said threshold level

6. A circuit for amplifying an input signal, comprising:

An amplifier;

means for controlling the gain of said amplifier's gain responsive to a control signal;

means for bypassing said amplifier when the gain of said amplifier is reduced to a threshold level.

7. The circuit of claim 5, wherein said gain control means changes bias conditions of said amplifier.

8. The circuit of claim 5, wherein said means for bypassing attenuates said input signal.

9. The circuit of claim 6, wherein said amplifier is inactivated when the gain of said amplifier is reduced to said threshold level.

10. A radio receiver, comprising:

means for receiving a signal to provide a received signal;

means for providing a control signal proportional to the strength of said received signal;

amplifying means for variably amplifying said received signal in response to said control signal, including means for bypassing said amplifying means when said control signal exceeds a threshold level.

11. The receiver of claim 8, wherein said control signal changes biasing condition of said amplifying means.

12. The receiver of claim 8, wherein said bypassing means attenuates the received signal.

13. The radio receiver of claim 10-, wherein said amplifier is inactivated when the gain of said amplifier is reduced to said threshold level.

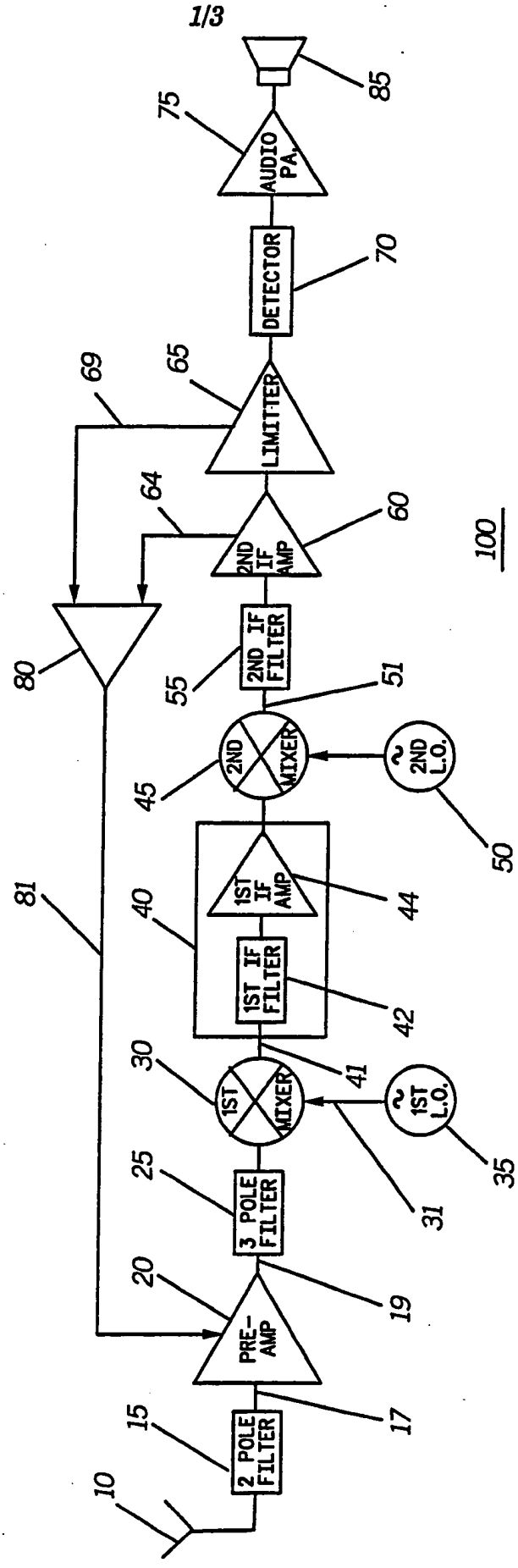

85
75
AUDIO PA.
DETECTOR
70
69
65
LIMITTER
64
2ND IF AMP
60
100
80
2ND IF FILTER
55
51
2ND MIXER
2ND L.O.
45
50
1ST IF AMP
44
81
40
1ST IF FILTER
42
30
41
1ST MIXER
1ST L.O.
35
31
25
3 POLE FILTER
20
19
PRE-AMP
17
15
2 POLE FILTER
10

FIG.1

FIG.2a

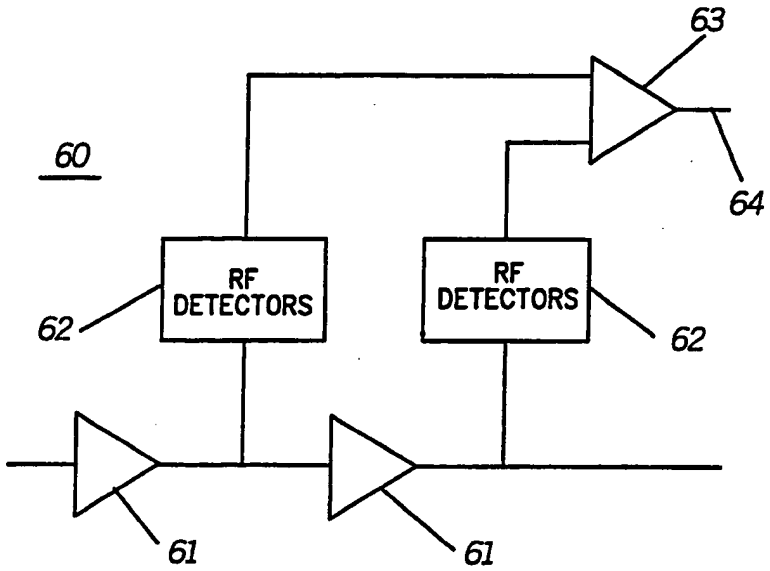
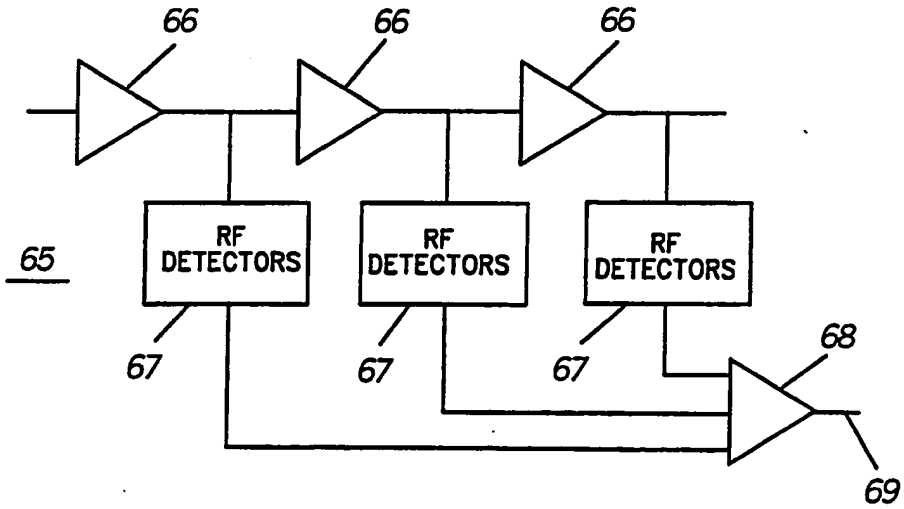

63
60
64
RF DETECTORS
RF DETECTORS
62
62
61
61

FIG.2b


66
66
66
65
RF DETECTORS
RF DETECTORS
RF DETECTORS
67
67
67
68
69

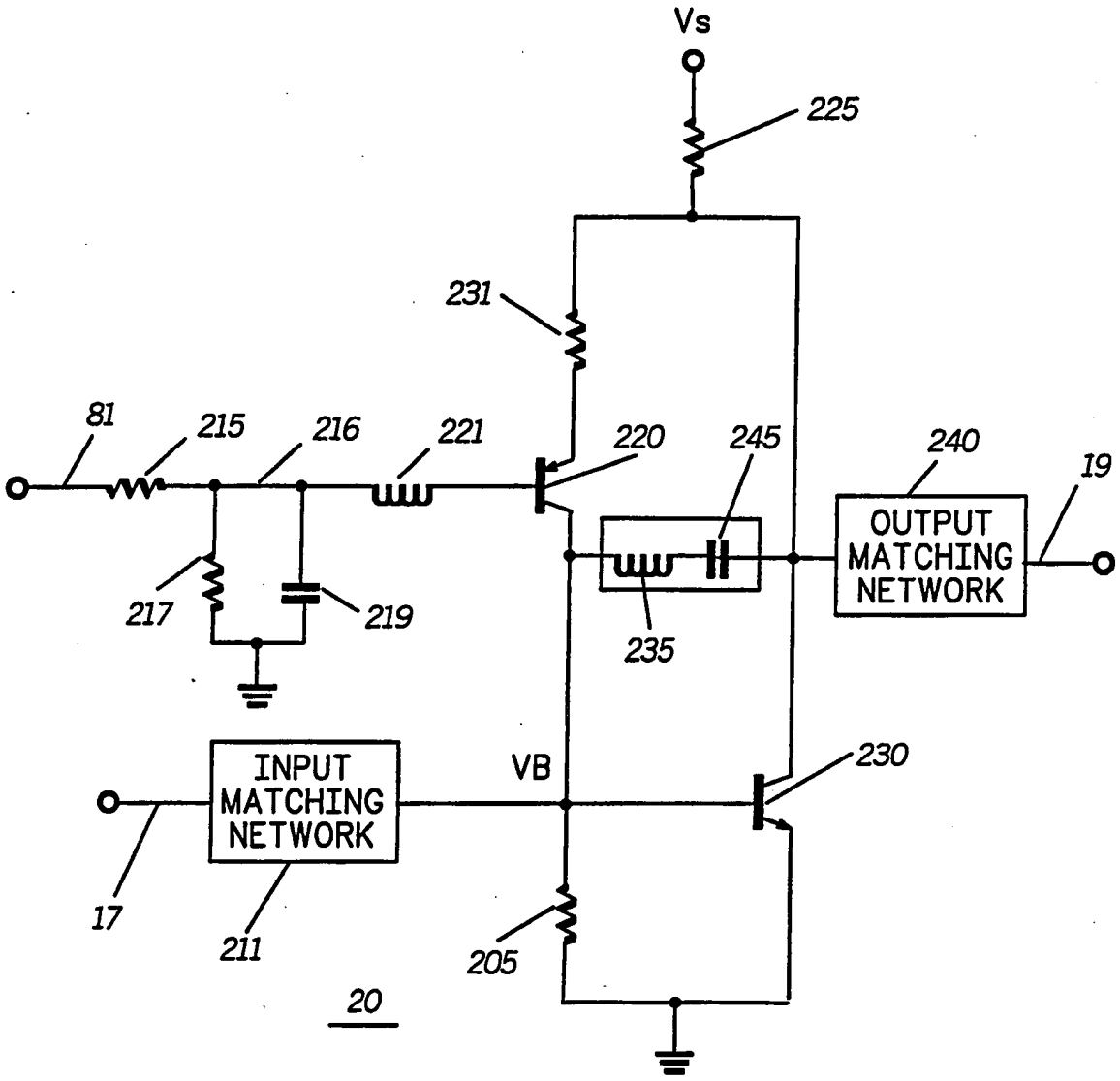

Vs
225
231
81
215
216
221
220
245
240
19
OUTPUT MATCHING NETWORK
217
219
235
INPUT MATCHING NETWORK
VB
230
17
211
205
20

FIG.3

INTERNATIONAL SEARCH REPORT

International Application No PCT/US90/02301

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [3]

According to International Patent Classification (IPC) or to both National Classification and IPC

INT. CL 5 H04B 1/06

U.S. CL: 455/241, 246, 295 330/284

II. FIELDS SEARCHED

Minimum Documentation Searched [4]

Classification System	Classification Symbols
U.S.	455/234, 241, 246, 247, 249, 295, 308 330/274, 284, 285

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [5]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [14]

Category *	Citation of Document, [16] with indication, where appropriate, of the relevant passages [17]	Relevant to Claim No. [18]
Y	US, A, 4,776,040, (ICHIKAWA ET AL,) 04 October 1988 See entire document.	1-13
Y,P	US, A, 4,850,038, (SHIBATA ET AL,) 18 July 1989 See entire document.	1-13
A,P	US, A, 4,939,788, (HASEGAWA) 03 July 1990	
A	US, A, 4,479,255, (GEESEN ET AL,) 23 October 1984	
A,P	US, A, 4,872,206, (GRAZIADEI ET AL,) 03 October 1989	

* Special categories of cited documents: [15]

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search [2]	Date of Mailing of this International Search Report [2]
09 AUGUST 1990	13 SEP 1990
International Searching Authority [1]	**Signature of Authorized Officer [20]**
ISA/US	CURTIS A. KUNTZ

Form PCT/ISA/210 (second sheet) (May 1986)